Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.070”**

**.035”**

**.0079”**

**.0089”**

**GATE**

**S**

**O**

**U**

**R**

**C**

**E**

**S**

**O**

**U**

**R**

**C**

**E**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .0079” X .0089” min.**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .035” X .070” DATE: 3/8/23**

**MFG: INT’L RECTIFIER THICKNESS .017” P/N: IRF7530**

**DG 10.1.2**

#### Rev B, 7/1